---------- Begin Simulation Statistics ----------

sim\_seconds 0.364964 # Number of seconds simulated

sim\_ticks 364964286500 # Number of ticks simulated

final\_tick 364964286500 # Number of ticks from beginning of simulation (restored from checkpoints and never reset)

sim\_freq 1000000000000 # Frequency of simulated ticks

host\_inst\_rate 321935 # Simulator instruction rate (inst/s)

host\_op\_rate 321935 # Simulator op (including micro ops) rate (op/s)

host\_tick\_rate 264132547 # Simulator tick rate (ticks/s)

host\_mem\_usage 644876 # Number of bytes of host memory used

host\_seconds 1381.75 # Real time elapsed on the host

sim\_insts 444833083 # Number of instructions simulated

sim\_ops 444833083 # Number of ops (including micro ops) simulated

system.voltage\_domain.voltage 1 # Voltage in Volts

system.clk\_domain.clock 1000 # Clock period in ticks

system.mem\_ctrls.pwrStateResidencyTicks::UNDEFINED 364964286500 # Cumulative time (in ticks) in various power states

system.mem\_ctrls.bytes\_read::.cpu.inst 178242240 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_read::.cpu.data 185792 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_read::total 178428032 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_inst\_read::.cpu.inst 178242240 # Number of instructions bytes read from this memory

system.mem\_ctrls.bytes\_inst\_read::total 178242240 # Number of instructions bytes read from this memory

system.mem\_ctrls.bytes\_written::.writebacks 21504 # Number of bytes written to this memory

system.mem\_ctrls.bytes\_written::total 21504 # Number of bytes written to this memory

system.mem\_ctrls.num\_reads::.cpu.inst 2785035 # Number of read requests responded to by this memory

system.mem\_ctrls.num\_reads::.cpu.data 2903 # Number of read requests responded to by this memory

system.mem\_ctrls.num\_reads::total 2787938 # Number of read requests responded to by this memory

system.mem\_ctrls.num\_writes::.writebacks 336 # Number of write requests responded to by this memory

system.mem\_ctrls.num\_writes::total 336 # Number of write requests responded to by this memory

system.mem\_ctrls.bw\_read::.cpu.inst 488382690 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_read::.cpu.data 509069 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_read::total 488891759 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_inst\_read::.cpu.inst 488382690 # Instruction read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_inst\_read::total 488382690 # Instruction read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_write::.writebacks 58921 # Write bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_write::total 58921 # Write bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_total::.writebacks 58921 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.bw\_total::.cpu.inst 488382690 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.bw\_total::.cpu.data 509069 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.bw\_total::total 488950680 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.avgPriority\_.writebacks::samples 2015144.00 # Average QoS priority value for accepted requests

system.mem\_ctrls.avgPriority\_.cpu.inst::samples 1117820.00 # Average QoS priority value for accepted requests

system.mem\_ctrls.avgPriority\_.cpu.data::samples 2806.00 # Average QoS priority value for accepted requests

system.mem\_ctrls.priorityMinLatency 0.000000018750 # per QoS priority minimum request to response latency (s)

system.mem\_ctrls.priorityMaxLatency 0.055103176750 # per QoS priority maximum request to response latency (s)

system.mem\_ctrls.numReadWriteTurnArounds 115013 # Number of turnarounds from READ to WRITE

system.mem\_ctrls.numWriteReadTurnArounds 115013 # Number of turnarounds from WRITE to READ

system.mem\_ctrls.numStayReadState 4948085 # Number of times bus staying in READ state

system.mem\_ctrls.numStayWriteState 1908436 # Number of times bus staying in WRITE state

system.mem\_ctrls.readReqs 2787939 # Number of read requests accepted

system.mem\_ctrls.writeReqs 2784861 # Number of write requests accepted

system.mem\_ctrls.readBursts 2787939 # Number of DRAM read bursts, including those serviced by the write queue

system.mem\_ctrls.writeBursts 2784861 # Number of DRAM write bursts, including those merged in the write queue

system.mem\_ctrls.bytesReadDRAM 71720064 # Total number of bytes read from DRAM

system.mem\_ctrls.bytesReadWrQ 106708032 # Total number of bytes read from write queue

system.mem\_ctrls.bytesWritten 128967872 # Total number of bytes written to DRAM

system.mem\_ctrls.bytesReadSys 178428096 # Total read bytes from the system interface side

system.mem\_ctrls.bytesWrittenSys 178231104 # Total written bytes from the system interface side

system.mem\_ctrls.servicedByWrQ 1667313 # Number of DRAM read bursts serviced by the write queue

system.mem\_ctrls.mergedWrBursts 769717 # Number of DRAM write bursts merged with an existing one

system.mem\_ctrls.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write

system.mem\_ctrls.perBankRdBursts::0 263999 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::1 71906 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::2 273759 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::3 42224 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::4 12191 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::5 3211 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::6 190931 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::7 32885 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::8 200 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::9 513 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::10 439 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::11 81 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::12 40303 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::13 22 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::14 112648 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::15 75314 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::0 518255 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::1 103183 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::2 484944 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::3 150223 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::4 12020 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::5 2792 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::6 232946 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::7 34909 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::8 40 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::9 55 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::10 20 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::11 62 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::12 42870 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::13 14 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::14 275263 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::15 157527 # Per bank write bursts

system.mem\_ctrls.numRdRetry 0 # Number of times read queue was full causing retry

system.mem\_ctrls.numWrRetry 0 # Number of times write queue was full causing retry

system.mem\_ctrls.totGap 364964279000 # Total gap between requests

system.mem\_ctrls.readPktSize::0 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::1 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::2 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::3 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::4 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::5 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::6 2787939 # Read request sizes (log2)

system.mem\_ctrls.writePktSize::0 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::1 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::2 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::3 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::4 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::5 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::6 2784861 # Write request sizes (log2)

system.mem\_ctrls.rdQLenPdf::0 1118851 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::1 1759 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::2 16 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::3 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::4 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::5 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::6 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::7 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::8 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::9 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::10 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::11 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::12 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::13 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::14 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::15 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::16 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::17 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::18 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::19 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::20 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::21 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::22 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::23 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::24 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::25 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::26 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::27 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::28 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::29 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::30 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::31 0 # What read queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::0 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::1 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::2 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::3 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::4 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::5 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::6 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::7 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::8 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::9 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::10 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::11 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::12 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::13 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::14 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::15 51759 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::16 54854 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::17 108371 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::18 122854 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::19 127587 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::20 117678 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::21 118548 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::22 124208 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::23 139971 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::24 119460 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::25 118188 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::26 120774 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::27 115137 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::28 115157 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::29 115089 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::30 115079 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::31 115053 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::32 115045 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::33 127 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::34 87 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::35 60 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::36 22 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::37 14 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::38 7 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::39 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::40 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::41 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::42 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::43 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::44 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::45 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::46 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::47 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::48 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::49 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::50 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::51 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::52 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::53 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::54 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::55 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::56 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::57 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::58 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::59 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::60 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::61 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::62 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::63 0 # What write queue length does an incoming req see

system.mem\_ctrls.bytesPerActivate::samples 501757 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::mean 399.966677 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::gmean 275.402804 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::stdev 311.175457 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::0-127 96305 19.19% 19.19% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::128-255 94083 18.75% 37.94% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::256-383 87544 17.45% 55.39% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::384-511 48102 9.59% 64.98% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::512-639 53838 10.73% 75.71% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::640-767 32081 6.39% 82.10% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::768-895 26336 5.25% 87.35% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::896-1023 16229 3.23% 90.59% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::1024-1151 47239 9.41% 100.00% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::total 501757 # Bytes accessed per row activation

system.mem\_ctrls.rdPerTurnAround::samples 115013 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::mean 9.743420 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::stdev 5.002090 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::0-15 94874 82.49% 82.49% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::16-31 20127 17.50% 99.99% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::32-47 7 0.01% 100.00% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::48-63 3 0.00% 100.00% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::96-111 1 0.00% 100.00% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::320-335 1 0.00% 100.00% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::total 115013 # Reads before turning the bus around for writes

system.mem\_ctrls.wrPerTurnAround::samples 115013 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::mean 17.520828 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::gmean 17.436953 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::stdev 1.747482 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::16 58791 51.12% 51.12% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::17 2369 2.06% 53.18% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::18 18021 15.67% 68.85% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::19 12377 10.76% 79.61% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::20 19459 16.92% 96.53% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::21 3297 2.87% 99.39% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::22 255 0.22% 99.61% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::23 182 0.16% 99.77% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::24 167 0.15% 99.92% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::25 59 0.05% 99.97% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::26 18 0.02% 99.98% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::27 15 0.01% 100.00% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::28 3 0.00% 100.00% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::total 115013 # Writes before turning the bus around for reads

system.mem\_ctrls.masterReadBytes::.cpu.inst 71540480 # Per-master bytes read from memory

system.mem\_ctrls.masterReadBytes::.cpu.data 179584 # Per-master bytes read from memory

system.mem\_ctrls.masterWriteBytes::.writebacks 128967872 # Per-master bytes write to memory

system.mem\_ctrls.masterReadRate::.cpu.inst 196020494.734078586102 # Per-master bytes read from memory rate (Bytes/sec)

system.mem\_ctrls.masterReadRate::.cpu.data 492059.104528300173 # Per-master bytes read from memory rate (Bytes/sec)

system.mem\_ctrls.masterWriteRate::.writebacks 353371211.295218050480 # Per-master bytes write to memory rate (Bytes/sec)

system.mem\_ctrls.masterReadAccesses::.cpu.inst 2785036 # Per-master read serviced memory accesses

system.mem\_ctrls.masterReadAccesses::.cpu.data 2903 # Per-master read serviced memory accesses

system.mem\_ctrls.masterWriteAccesses::.writebacks 2784861 # Per-master write serviced memory accesses

system.mem\_ctrls.masterReadTotalLat::.cpu.inst 39664286750 # Per-master read total memory access latency

system.mem\_ctrls.masterReadTotalLat::.cpu.data 126340000 # Per-master read total memory access latency

system.mem\_ctrls.masterWriteTotalLat::.writebacks 8861220676000 # Per-master write total memory access latency

system.mem\_ctrls.masterReadAvgLat::.cpu.inst 14241.93 # Per-master read average memory access latency

system.mem\_ctrls.masterReadAvgLat::.cpu.data 43520.50 # Per-master read average memory access latency

system.mem\_ctrls.masterWriteAvgLat::.writebacks 3181925.66 # Per-master write average memory access latency

system.mem\_ctrls.totQLat 18778889250 # Total ticks spent queuing

system.mem\_ctrls.totMemAccLat 39790626750 # Total ticks spent from burst creation until serviced by the DRAM

system.mem\_ctrls.totBusLat 5603130000 # Total ticks spent in databus transfers

system.mem\_ctrls.avgQLat 16757.50 # Average queueing delay per DRAM burst

system.mem\_ctrls.avgBusLat 5000.00 # Average bus latency per DRAM burst

system.mem\_ctrls.avgMemAccLat 35507.50 # Average memory access latency per DRAM burst

system.mem\_ctrls.avgRdBW 196.51 # Average DRAM read bandwidth in MiByte/s

system.mem\_ctrls.avgWrBW 353.37 # Average achieved write bandwidth in MiByte/s

system.mem\_ctrls.avgRdBWSys 488.89 # Average system read bandwidth in MiByte/s

system.mem\_ctrls.avgWrBWSys 488.35 # Average system write bandwidth in MiByte/s

system.mem\_ctrls.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s

system.mem\_ctrls.busUtil 4.30 # Data bus utilization in percentage

system.mem\_ctrls.busUtilRead 1.54 # Data bus utilization in percentage for reads

system.mem\_ctrls.busUtilWrite 2.76 # Data bus utilization in percentage for writes

system.mem\_ctrls.avgRdQLen 1.00 # Average read queue length when enqueuing

system.mem\_ctrls.avgWrQLen 25.06 # Average write queue length when enqueuing

system.mem\_ctrls.readRowHits 908855 # Number of row buffer hits during reads

system.mem\_ctrls.writeRowHits 1725129 # Number of row buffer hits during writes

system.mem\_ctrls.readRowHitRate 81.10 # Row buffer hit rate for reads

system.mem\_ctrls.writeRowHitRate 85.61 # Row buffer hit rate for writes

system.mem\_ctrls.avgGap 65490.29 # Average gap between requests

system.mem\_ctrls.pageHitRate 84.00 # Row buffer hit rate, read and write combined

system.mem\_ctrls\_0.actEnergy 2908400460 # Energy for activate commands per rank (pJ)

system.mem\_ctrls\_0.preEnergy 1545847710 # Energy for precharge commands per rank (pJ)

system.mem\_ctrls\_0.readEnergy 6362489700 # Energy for read commands per rank (pJ)

system.mem\_ctrls\_0.writeEnergy 8034999840 # Energy for write commands per rank (pJ)

system.mem\_ctrls\_0.refreshEnergy 26324416560.000004 # Energy for refresh commands per rank (pJ)

system.mem\_ctrls\_0.actBackEnergy 54224495580 # Energy for active background per rank (pJ)

system.mem\_ctrls\_0.preBackEnergy 587609280 # Energy for precharge background per rank (pJ)

system.mem\_ctrls\_0.actPowerDownEnergy 84042266610 # Energy for active power-down per rank (pJ)

system.mem\_ctrls\_0.prePowerDownEnergy 11057346720 # Energy for precharge power-down per rank (pJ)

system.mem\_ctrls\_0.selfRefreshEnergy 7690456200 # Energy for self refresh per rank (pJ)

system.mem\_ctrls\_0.totalEnergy 202782909270 # Total energy per rank (pJ)

system.mem\_ctrls\_0.averagePower 555.623980 # Core power per rank (mW)

system.mem\_ctrls\_0.totalIdleTime 244507163750 # Total Idle time Per DRAM Rank

system.mem\_ctrls\_0.memoryStateTime::IDLE 313502500 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::REF 11135540000 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::SREF 31412070000 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::PRE\_PDN 28797601750 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::ACT 109008080250 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::ACT\_PDN 184297492000 # Time in different power states

system.mem\_ctrls\_1.actEnergy 674201640 # Energy for activate commands per rank (pJ)

system.mem\_ctrls\_1.preEnergy 358320105 # Energy for precharge commands per rank (pJ)

system.mem\_ctrls\_1.readEnergy 1638772800 # Energy for read commands per rank (pJ)

system.mem\_ctrls\_1.writeEnergy 2483942220 # Energy for write commands per rank (pJ)

system.mem\_ctrls\_1.refreshEnergy 25610204880.000004 # Energy for refresh commands per rank (pJ)

system.mem\_ctrls\_1.actBackEnergy 51779563230 # Energy for active background per rank (pJ)

system.mem\_ctrls\_1.preBackEnergy 1224196800 # Energy for precharge background per rank (pJ)

system.mem\_ctrls\_1.actPowerDownEnergy 49157289060 # Energy for active power-down per rank (pJ)

system.mem\_ctrls\_1.prePowerDownEnergy 38753801280 # Energy for precharge power-down per rank (pJ)

system.mem\_ctrls\_1.selfRefreshEnergy 11626525740 # Energy for self refresh per rank (pJ)

system.mem\_ctrls\_1.totalEnergy 183327315735 # Total energy per rank (pJ)

system.mem\_ctrls\_1.averagePower 502.315768 # Core power per rank (mW)

system.mem\_ctrls\_1.totalIdleTime 248178157000 # Total Idle time Per DRAM Rank

system.mem\_ctrls\_1.memoryStateTime::IDLE 2125532500 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::REF 10833420000 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::SREF 39456495750 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::PRE\_PDN 100921072250 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::ACT 103826740500 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::ACT\_PDN 107801025500 # Time in different power states

system.pwrStateResidencyTicks::UNDEFINED 364964286500 # Cumulative time (in ticks) in various power states

system.cpu.branchPred.lookups 67948048 # Number of BP lookups

system.cpu.branchPred.condPredicted 48993783 # Number of conditional branches predicted

system.cpu.branchPred.condIncorrect 1559861 # Number of conditional branches incorrect

system.cpu.branchPred.BTBLookups 50549888 # Number of BTB lookups

system.cpu.branchPred.BTBHits 43954068 # Number of BTB hits

system.cpu.branchPred.BTBCorrect 0 # Number of correct BTB predictions (this stat may not work properly.

system.cpu.branchPred.BTBHitPct 86.951860 # BTB Hit Percentage

system.cpu.branchPred.usedRAS 6334763 # Number of times the RAS was used to get a target.

system.cpu.branchPred.RASInCorrect 20 # Number of incorrect RAS predictions.

system.cpu.branchPred.indirectLookups 1739590 # Number of indirect predictor lookups.

system.cpu.branchPred.indirectHits 1723289 # Number of indirect target hits.

system.cpu.branchPred.indirectMisses 16301 # Number of indirect misses.

system.cpu.branchPredindirectMispredicted 167665 # Number of mispredicted indirect branches.

system.cpu\_voltage\_domain.voltage 1 # Voltage in Volts

system.cpu\_clk\_domain.clock 500 # Clock period in ticks

system.cpu.dtb.fetch\_hits 0 # ITB hits

system.cpu.dtb.fetch\_misses 0 # ITB misses

system.cpu.dtb.fetch\_acv 0 # ITB acv

system.cpu.dtb.fetch\_accesses 0 # ITB accesses

system.cpu.dtb.read\_hits 72221068 # DTB read hits

system.cpu.dtb.read\_misses 32 # DTB read misses

system.cpu.dtb.read\_acv 0 # DTB read access violations

system.cpu.dtb.read\_accesses 72221100 # DTB read accesses

system.cpu.dtb.write\_hits 39293985 # DTB write hits

system.cpu.dtb.write\_misses 6 # DTB write misses

system.cpu.dtb.write\_acv 2 # DTB write access violations

system.cpu.dtb.write\_accesses 39293991 # DTB write accesses

system.cpu.dtb.data\_hits 111515053 # DTB hits

system.cpu.dtb.data\_misses 38 # DTB misses

system.cpu.dtb.data\_acv 2 # DTB access violations

system.cpu.dtb.data\_accesses 111515091 # DTB accesses

system.cpu.itb.fetch\_hits 146977066 # ITB hits

system.cpu.itb.fetch\_misses 38 # ITB misses

system.cpu.itb.fetch\_acv 0 # ITB acv

system.cpu.itb.fetch\_accesses 146977104 # ITB accesses

system.cpu.itb.read\_hits 0 # DTB read hits

system.cpu.itb.read\_misses 0 # DTB read misses

system.cpu.itb.read\_acv 0 # DTB read access violations

system.cpu.itb.read\_accesses 0 # DTB read accesses

system.cpu.itb.write\_hits 0 # DTB write hits

system.cpu.itb.write\_misses 0 # DTB write misses

system.cpu.itb.write\_acv 0 # DTB write access violations

system.cpu.itb.write\_accesses 0 # DTB write accesses

system.cpu.itb.data\_hits 0 # DTB hits

system.cpu.itb.data\_misses 0 # DTB misses

system.cpu.itb.data\_acv 0 # DTB access violations

system.cpu.itb.data\_accesses 0 # DTB accesses

system.cpu.workload.numSyscalls 167539 # Number of system calls

system.cpu.pwrStateResidencyTicks::ON 364964286500 # Cumulative time (in ticks) in various power states

system.cpu.numCycles 729928573 # number of cpu cycles simulated

system.cpu.numWorkItemsStarted 0 # number of work items this cpu started

system.cpu.numWorkItemsCompleted 0 # number of work items this cpu completed

system.cpu.committedInsts 444833083 # Number of instructions committed

system.cpu.committedOps 444833083 # Number of ops (including micro ops) committed

system.cpu.discardedOps 2904253 # Number of ops (including micro ops) which were discarded before commit

system.cpu.numFetchSuspends 0 # Number of times Execute suspended instruction fetching

system.cpu.cpi 1.640904 # CPI: cycles per instruction

system.cpu.ipc 0.609420 # IPC: instructions per cycle

system.cpu.op\_class\_0::No\_OpClass 8646356 1.94% 1.94% # Class of committed instruction

system.cpu.op\_class\_0::IntAlu 321159161 72.20% 74.14% # Class of committed instruction

system.cpu.op\_class\_0::IntMult 2406685 0.54% 74.68% # Class of committed instruction

system.cpu.op\_class\_0::IntDiv 0 0.00% 74.68% # Class of committed instruction

system.cpu.op\_class\_0::FloatAdd 897130 0.20% 74.88% # Class of committed instruction

system.cpu.op\_class\_0::FloatCmp 191234 0.04% 74.93% # Class of committed instruction

system.cpu.op\_class\_0::FloatCvt 281149 0.06% 74.99% # Class of committed instruction

system.cpu.op\_class\_0::FloatMult 204955 0.05% 75.04% # Class of committed instruction

system.cpu.op\_class\_0::FloatMultAcc 0 0.00% 75.04% # Class of committed instruction

system.cpu.op\_class\_0::FloatDiv 60615 0.01% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::FloatMisc 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::FloatSqrt 4361 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdAdd 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdAddAcc 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdAlu 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdCmp 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdCvt 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdMisc 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdMult 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdMultAcc 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdShift 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdShiftAcc 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdSqrt 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatAdd 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatAlu 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatCmp 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatCvt 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatDiv 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatMisc 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatMult 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatMultAcc 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdFloatSqrt 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdAes 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdAesMix 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdSha1Hash 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdSha1Hash2 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdSha256Hash 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdSha256Hash2 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdShaSigma2 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::SimdShaSigma3 0 0.00% 75.05% # Class of committed instruction

system.cpu.op\_class\_0::MemRead 71215571 16.01% 91.06% # Class of committed instruction

system.cpu.op\_class\_0::MemWrite 38336246 8.62% 99.68% # Class of committed instruction

system.cpu.op\_class\_0::FloatMemRead 573072 0.13% 99.81% # Class of committed instruction

system.cpu.op\_class\_0::FloatMemWrite 856548 0.19% 100.00% # Class of committed instruction

system.cpu.op\_class\_0::IprAccess 0 0.00% 100.00% # Class of committed instruction

system.cpu.op\_class\_0::InstPrefetch 0 0.00% 100.00% # Class of committed instruction

system.cpu.op\_class\_0::total 444833083 # Class of committed instruction

system.cpu.tickCycles 521790612 # Number of cycles that the object actually ticked

system.cpu.idleCycles 208137961 # Total number of cycles that the object has spent stopped

system.cpu.fetch2.int\_instructions 324781794 # Number of integer instructions successfully decoded

system.cpu.fetch2.fp\_instructions 1655770 # Number of floating point instructions successfully decoded

system.cpu.fetch2.vec\_instructions 0 # Number of SIMD instructions successfully decoded

system.cpu.fetch2.load\_instructions 75288467 # Number of memory load instructions successfully decoded

system.cpu.fetch2.store\_instructions 40779041 # Number of memory store instructions successfully decoded

system.cpu.dcache.tags.pwrStateResidencyTicks::UNDEFINED 364964286500 # Cumulative time (in ticks) in various power states

system.cpu.dcache.tags.tagsinuse 976.465421 # Cycle average of tags in use

system.cpu.dcache.tags.total\_refs 110991178 # Total number of references to valid blocks.

system.cpu.dcache.tags.sampled\_refs 2903 # Sample count of references to valid blocks.

system.cpu.dcache.tags.avg\_refs 38233.268343 # Average number of references to valid blocks.

system.cpu.dcache.tags.warmup\_cycle 206000 # Cycle when the warmup percentage was hit.

system.cpu.dcache.tags.occ\_blocks::.cpu.data 976.465421 # Average occupied blocks per requestor

system.cpu.dcache.tags.occ\_percent::.cpu.data 0.953580 # Average percentage of cache occupancy

system.cpu.dcache.tags.occ\_percent::total 0.953580 # Average percentage of cache occupancy

system.cpu.dcache.tags.occ\_task\_id\_blocks::1024 1000 # Occupied blocks per task id

system.cpu.dcache.tags.age\_task\_id\_blocks\_1024::0 17 # Occupied blocks per task id

system.cpu.dcache.tags.age\_task\_id\_blocks\_1024::4 983 # Occupied blocks per task id

system.cpu.dcache.tags.occ\_task\_id\_percent::1024 0.976562 # Percentage of cache occupancy per task id

system.cpu.dcache.tags.tag\_accesses 221985643 # Number of tag accesses

system.cpu.dcache.tags.data\_accesses 221985643 # Number of data accesses

system.cpu.dcache.pwrStateResidencyTicks::UNDEFINED 364964286500 # Cumulative time (in ticks) in various power states

system.cpu.dcache.ReadReq\_hits::.cpu.data 71641647 # number of ReadReq hits

system.cpu.dcache.ReadReq\_hits::total 71641647 # number of ReadReq hits

system.cpu.dcache.WriteReq\_hits::.cpu.data 39038046 # number of WriteReq hits

system.cpu.dcache.WriteReq\_hits::total 39038046 # number of WriteReq hits

system.cpu.dcache.LoadLockedReq\_hits::.cpu.data 154290 # number of LoadLockedReq hits

system.cpu.dcache.LoadLockedReq\_hits::total 154290 # number of LoadLockedReq hits

system.cpu.dcache.StoreCondReq\_hits::.cpu.data 154292 # number of StoreCondReq hits

system.cpu.dcache.StoreCondReq\_hits::total 154292 # number of StoreCondReq hits

system.cpu.dcache.demand\_hits::.cpu.data 110679693 # number of demand (read+write) hits

system.cpu.dcache.demand\_hits::total 110679693 # number of demand (read+write) hits

system.cpu.dcache.overall\_hits::.cpu.data 110679693 # number of overall hits

system.cpu.dcache.overall\_hits::total 110679693 # number of overall hits

system.cpu.dcache.ReadReq\_misses::.cpu.data 2643 # number of ReadReq misses

system.cpu.dcache.ReadReq\_misses::total 2643 # number of ReadReq misses

system.cpu.dcache.WriteReq\_misses::.cpu.data 450 # number of WriteReq misses

system.cpu.dcache.WriteReq\_misses::total 450 # number of WriteReq misses

system.cpu.dcache.LoadLockedReq\_misses::.cpu.data 2 # number of LoadLockedReq misses

system.cpu.dcache.LoadLockedReq\_misses::total 2 # number of LoadLockedReq misses

system.cpu.dcache.demand\_misses::.cpu.data 3093 # number of demand (read+write) misses

system.cpu.dcache.demand\_misses::total 3093 # number of demand (read+write) misses

system.cpu.dcache.overall\_misses::.cpu.data 3093 # number of overall misses

system.cpu.dcache.overall\_misses::total 3093 # number of overall misses

system.cpu.dcache.ReadReq\_miss\_latency::.cpu.data 202692500 # number of ReadReq miss cycles

system.cpu.dcache.ReadReq\_miss\_latency::total 202692500 # number of ReadReq miss cycles

system.cpu.dcache.WriteReq\_miss\_latency::.cpu.data 29585000 # number of WriteReq miss cycles

system.cpu.dcache.WriteReq\_miss\_latency::total 29585000 # number of WriteReq miss cycles

system.cpu.dcache.LoadLockedReq\_miss\_latency::.cpu.data 119500 # number of LoadLockedReq miss cycles

system.cpu.dcache.LoadLockedReq\_miss\_latency::total 119500 # number of LoadLockedReq miss cycles

system.cpu.dcache.demand\_miss\_latency::.cpu.data 232277500 # number of demand (read+write) miss cycles

system.cpu.dcache.demand\_miss\_latency::total 232277500 # number of demand (read+write) miss cycles

system.cpu.dcache.overall\_miss\_latency::.cpu.data 232277500 # number of overall miss cycles

system.cpu.dcache.overall\_miss\_latency::total 232277500 # number of overall miss cycles

system.cpu.dcache.ReadReq\_accesses::.cpu.data 71644290 # number of ReadReq accesses(hits+misses)

system.cpu.dcache.ReadReq\_accesses::total 71644290 # number of ReadReq accesses(hits+misses)

system.cpu.dcache.WriteReq\_accesses::.cpu.data 39038496 # number of WriteReq accesses(hits+misses)

system.cpu.dcache.WriteReq\_accesses::total 39038496 # number of WriteReq accesses(hits+misses)

system.cpu.dcache.LoadLockedReq\_accesses::.cpu.data 154292 # number of LoadLockedReq accesses(hits+misses)

system.cpu.dcache.LoadLockedReq\_accesses::total 154292 # number of LoadLockedReq accesses(hits+misses)

system.cpu.dcache.StoreCondReq\_accesses::.cpu.data 154292 # number of StoreCondReq accesses(hits+misses)

system.cpu.dcache.StoreCondReq\_accesses::total 154292 # number of StoreCondReq accesses(hits+misses)

system.cpu.dcache.demand\_accesses::.cpu.data 110682786 # number of demand (read+write) accesses

system.cpu.dcache.demand\_accesses::total 110682786 # number of demand (read+write) accesses

system.cpu.dcache.overall\_accesses::.cpu.data 110682786 # number of overall (read+write) accesses

system.cpu.dcache.overall\_accesses::total 110682786 # number of overall (read+write) accesses

system.cpu.dcache.ReadReq\_miss\_rate::.cpu.data 0.000037 # miss rate for ReadReq accesses

system.cpu.dcache.ReadReq\_miss\_rate::total 0.000037 # miss rate for ReadReq accesses

system.cpu.dcache.WriteReq\_miss\_rate::.cpu.data 0.000012 # miss rate for WriteReq accesses

system.cpu.dcache.WriteReq\_miss\_rate::total 0.000012 # miss rate for WriteReq accesses

system.cpu.dcache.LoadLockedReq\_miss\_rate::.cpu.data 0.000013 # miss rate for LoadLockedReq accesses

system.cpu.dcache.LoadLockedReq\_miss\_rate::total 0.000013 # miss rate for LoadLockedReq accesses

system.cpu.dcache.demand\_miss\_rate::.cpu.data 0.000028 # miss rate for demand accesses

system.cpu.dcache.demand\_miss\_rate::total 0.000028 # miss rate for demand accesses

system.cpu.dcache.overall\_miss\_rate::.cpu.data 0.000028 # miss rate for overall accesses

system.cpu.dcache.overall\_miss\_rate::total 0.000028 # miss rate for overall accesses

system.cpu.dcache.ReadReq\_avg\_miss\_latency::.cpu.data 76690.314037 # average ReadReq miss latency

system.cpu.dcache.ReadReq\_avg\_miss\_latency::total 76690.314037 # average ReadReq miss latency

system.cpu.dcache.WriteReq\_avg\_miss\_latency::.cpu.data 65744.444444 # average WriteReq miss latency

system.cpu.dcache.WriteReq\_avg\_miss\_latency::total 65744.444444 # average WriteReq miss latency

system.cpu.dcache.LoadLockedReq\_avg\_miss\_latency::.cpu.data 59750 # average LoadLockedReq miss latency

system.cpu.dcache.LoadLockedReq\_avg\_miss\_latency::total 59750 # average LoadLockedReq miss latency

system.cpu.dcache.demand\_avg\_miss\_latency::.cpu.data 75097.801487 # average overall miss latency

system.cpu.dcache.demand\_avg\_miss\_latency::total 75097.801487 # average overall miss latency

system.cpu.dcache.overall\_avg\_miss\_latency::.cpu.data 75097.801487 # average overall miss latency

system.cpu.dcache.overall\_avg\_miss\_latency::total 75097.801487 # average overall miss latency

system.cpu.dcache.blocked\_cycles::no\_mshrs 0 # number of cycles access was blocked

system.cpu.dcache.blocked\_cycles::no\_targets 0 # number of cycles access was blocked

system.cpu.dcache.blocked::no\_mshrs 0 # number of cycles access was blocked

system.cpu.dcache.blocked::no\_targets 0 # number of cycles access was blocked

system.cpu.dcache.avg\_blocked\_cycles::no\_mshrs nan # average number of cycles each access was blocked

system.cpu.dcache.avg\_blocked\_cycles::no\_targets nan # average number of cycles each access was blocked

system.cpu.dcache.writebacks::.writebacks 336 # number of writebacks

system.cpu.dcache.writebacks::total 336 # number of writebacks

system.cpu.dcache.ReadReq\_mshr\_hits::.cpu.data 46 # number of ReadReq MSHR hits

system.cpu.dcache.ReadReq\_mshr\_hits::total 46 # number of ReadReq MSHR hits

system.cpu.dcache.WriteReq\_mshr\_hits::.cpu.data 146 # number of WriteReq MSHR hits

system.cpu.dcache.WriteReq\_mshr\_hits::total 146 # number of WriteReq MSHR hits

system.cpu.dcache.demand\_mshr\_hits::.cpu.data 192 # number of demand (read+write) MSHR hits

system.cpu.dcache.demand\_mshr\_hits::total 192 # number of demand (read+write) MSHR hits

system.cpu.dcache.overall\_mshr\_hits::.cpu.data 192 # number of overall MSHR hits

system.cpu.dcache.overall\_mshr\_hits::total 192 # number of overall MSHR hits

system.cpu.dcache.ReadReq\_mshr\_misses::.cpu.data 2597 # number of ReadReq MSHR misses

system.cpu.dcache.ReadReq\_mshr\_misses::total 2597 # number of ReadReq MSHR misses

system.cpu.dcache.WriteReq\_mshr\_misses::.cpu.data 304 # number of WriteReq MSHR misses

system.cpu.dcache.WriteReq\_mshr\_misses::total 304 # number of WriteReq MSHR misses

system.cpu.dcache.LoadLockedReq\_mshr\_misses::.cpu.data 2 # number of LoadLockedReq MSHR misses

system.cpu.dcache.LoadLockedReq\_mshr\_misses::total 2 # number of LoadLockedReq MSHR misses

system.cpu.dcache.demand\_mshr\_misses::.cpu.data 2901 # number of demand (read+write) MSHR misses

system.cpu.dcache.demand\_mshr\_misses::total 2901 # number of demand (read+write) MSHR misses

system.cpu.dcache.overall\_mshr\_misses::.cpu.data 2901 # number of overall MSHR misses

system.cpu.dcache.overall\_mshr\_misses::total 2901 # number of overall MSHR misses

system.cpu.dcache.ReadReq\_mshr\_miss\_latency::.cpu.data 198284500 # number of ReadReq MSHR miss cycles

system.cpu.dcache.ReadReq\_mshr\_miss\_latency::total 198284500 # number of ReadReq MSHR miss cycles

system.cpu.dcache.WriteReq\_mshr\_miss\_latency::.cpu.data 19658000 # number of WriteReq MSHR miss cycles

system.cpu.dcache.WriteReq\_mshr\_miss\_latency::total 19658000 # number of WriteReq MSHR miss cycles

system.cpu.dcache.LoadLockedReq\_mshr\_miss\_latency::.cpu.data 117500 # number of LoadLockedReq MSHR miss cycles

system.cpu.dcache.LoadLockedReq\_mshr\_miss\_latency::total 117500 # number of LoadLockedReq MSHR miss cycles

system.cpu.dcache.demand\_mshr\_miss\_latency::.cpu.data 217942500 # number of demand (read+write) MSHR miss cycles

system.cpu.dcache.demand\_mshr\_miss\_latency::total 217942500 # number of demand (read+write) MSHR miss cycles

system.cpu.dcache.overall\_mshr\_miss\_latency::.cpu.data 217942500 # number of overall MSHR miss cycles

system.cpu.dcache.overall\_mshr\_miss\_latency::total 217942500 # number of overall MSHR miss cycles

system.cpu.dcache.ReadReq\_mshr\_miss\_rate::.cpu.data 0.000036 # mshr miss rate for ReadReq accesses

system.cpu.dcache.ReadReq\_mshr\_miss\_rate::total 0.000036 # mshr miss rate for ReadReq accesses

system.cpu.dcache.WriteReq\_mshr\_miss\_rate::.cpu.data 0.000008 # mshr miss rate for WriteReq accesses

system.cpu.dcache.WriteReq\_mshr\_miss\_rate::total 0.000008 # mshr miss rate for WriteReq accesses

system.cpu.dcache.LoadLockedReq\_mshr\_miss\_rate::.cpu.data 0.000013 # mshr miss rate for LoadLockedReq accesses

system.cpu.dcache.LoadLockedReq\_mshr\_miss\_rate::total 0.000013 # mshr miss rate for LoadLockedReq accesses

system.cpu.dcache.demand\_mshr\_miss\_rate::.cpu.data 0.000026 # mshr miss rate for demand accesses

system.cpu.dcache.demand\_mshr\_miss\_rate::total 0.000026 # mshr miss rate for demand accesses

system.cpu.dcache.overall\_mshr\_miss\_rate::.cpu.data 0.000026 # mshr miss rate for overall accesses

system.cpu.dcache.overall\_mshr\_miss\_rate::total 0.000026 # mshr miss rate for overall accesses

system.cpu.dcache.ReadReq\_avg\_mshr\_miss\_latency::.cpu.data 76351.366962 # average ReadReq mshr miss latency

system.cpu.dcache.ReadReq\_avg\_mshr\_miss\_latency::total 76351.366962 # average ReadReq mshr miss latency

system.cpu.dcache.WriteReq\_avg\_mshr\_miss\_latency::.cpu.data 64664.473684 # average WriteReq mshr miss latency

system.cpu.dcache.WriteReq\_avg\_mshr\_miss\_latency::total 64664.473684 # average WriteReq mshr miss latency

system.cpu.dcache.LoadLockedReq\_avg\_mshr\_miss\_latency::.cpu.data 58750 # average LoadLockedReq mshr miss latency

system.cpu.dcache.LoadLockedReq\_avg\_mshr\_miss\_latency::total 58750 # average LoadLockedReq mshr miss latency

system.cpu.dcache.demand\_avg\_mshr\_miss\_latency::.cpu.data 75126.680455 # average overall mshr miss latency

system.cpu.dcache.demand\_avg\_mshr\_miss\_latency::total 75126.680455 # average overall mshr miss latency

system.cpu.dcache.overall\_avg\_mshr\_miss\_latency::.cpu.data 75126.680455 # average overall mshr miss latency

system.cpu.dcache.overall\_avg\_mshr\_miss\_latency::total 75126.680455 # average overall mshr miss latency

system.cpu.dcache.replacements 1903 # number of replacements

system.cpu.icache.tags.pwrStateResidencyTicks::UNDEFINED 364964286500 # Cumulative time (in ticks) in various power states

system.cpu.icache.tags.tagsinuse 508.536940 # Cycle average of tags in use

system.cpu.icache.tags.total\_refs 146977065 # Total number of references to valid blocks.

system.cpu.icache.tags.sampled\_refs 2785035 # Sample count of references to valid blocks.

system.cpu.icache.tags.avg\_refs 52.773866 # Average number of references to valid blocks.

system.cpu.icache.tags.warmup\_cycle 77000 # Cycle when the warmup percentage was hit.

system.cpu.icache.tags.occ\_blocks::.cpu.inst 508.536940 # Average occupied blocks per requestor

system.cpu.icache.tags.occ\_percent::.cpu.inst 0.993236 # Average percentage of cache occupancy

system.cpu.icache.tags.occ\_percent::total 0.993236 # Average percentage of cache occupancy

system.cpu.icache.tags.occ\_task\_id\_blocks::1024 510 # Occupied blocks per task id

system.cpu.icache.tags.age\_task\_id\_blocks\_1024::0 104 # Occupied blocks per task id

system.cpu.icache.tags.age\_task\_id\_blocks\_1024::1 3 # Occupied blocks per task id

system.cpu.icache.tags.age\_task\_id\_blocks\_1024::4 403 # Occupied blocks per task id

system.cpu.icache.tags.occ\_task\_id\_percent::1024 0.996094 # Percentage of cache occupancy per task id

system.cpu.icache.tags.tag\_accesses 296739167 # Number of tag accesses

system.cpu.icache.tags.data\_accesses 296739167 # Number of data accesses

system.cpu.icache.pwrStateResidencyTicks::UNDEFINED 364964286500 # Cumulative time (in ticks) in various power states

system.cpu.icache.ReadReq\_hits::.cpu.inst 144192030 # number of ReadReq hits

system.cpu.icache.ReadReq\_hits::total 144192030 # number of ReadReq hits

system.cpu.icache.demand\_hits::.cpu.inst 144192030 # number of demand (read+write) hits

system.cpu.icache.demand\_hits::total 144192030 # number of demand (read+write) hits

system.cpu.icache.overall\_hits::.cpu.inst 144192030 # number of overall hits

system.cpu.icache.overall\_hits::total 144192030 # number of overall hits

system.cpu.icache.ReadReq\_misses::.cpu.inst 2785036 # number of ReadReq misses

system.cpu.icache.ReadReq\_misses::total 2785036 # number of ReadReq misses

system.cpu.icache.demand\_misses::.cpu.inst 2785036 # number of demand (read+write) misses

system.cpu.icache.demand\_misses::total 2785036 # number of demand (read+write) misses

system.cpu.icache.overall\_misses::.cpu.inst 2785036 # number of overall misses

system.cpu.icache.overall\_misses::total 2785036 # number of overall misses

system.cpu.icache.ReadReq\_miss\_latency::.cpu.inst 116212332000 # number of ReadReq miss cycles

system.cpu.icache.ReadReq\_miss\_latency::total 116212332000 # number of ReadReq miss cycles

system.cpu.icache.demand\_miss\_latency::.cpu.inst 116212332000 # number of demand (read+write) miss cycles

system.cpu.icache.demand\_miss\_latency::total 116212332000 # number of demand (read+write) miss cycles

system.cpu.icache.overall\_miss\_latency::.cpu.inst 116212332000 # number of overall miss cycles

system.cpu.icache.overall\_miss\_latency::total 116212332000 # number of overall miss cycles

system.cpu.icache.ReadReq\_accesses::.cpu.inst 146977066 # number of ReadReq accesses(hits+misses)

system.cpu.icache.ReadReq\_accesses::total 146977066 # number of ReadReq accesses(hits+misses)

system.cpu.icache.demand\_accesses::.cpu.inst 146977066 # number of demand (read+write) accesses

system.cpu.icache.demand\_accesses::total 146977066 # number of demand (read+write) accesses

system.cpu.icache.overall\_accesses::.cpu.inst 146977066 # number of overall (read+write) accesses

system.cpu.icache.overall\_accesses::total 146977066 # number of overall (read+write) accesses

system.cpu.icache.ReadReq\_miss\_rate::.cpu.inst 0.018949 # miss rate for ReadReq accesses

system.cpu.icache.ReadReq\_miss\_rate::total 0.018949 # miss rate for ReadReq accesses

system.cpu.icache.demand\_miss\_rate::.cpu.inst 0.018949 # miss rate for demand accesses

system.cpu.icache.demand\_miss\_rate::total 0.018949 # miss rate for demand accesses

system.cpu.icache.overall\_miss\_rate::.cpu.inst 0.018949 # miss rate for overall accesses

system.cpu.icache.overall\_miss\_rate::total 0.018949 # miss rate for overall accesses

system.cpu.icache.ReadReq\_avg\_miss\_latency::.cpu.inst 41727.407473 # average ReadReq miss latency

system.cpu.icache.ReadReq\_avg\_miss\_latency::total 41727.407473 # average ReadReq miss latency

system.cpu.icache.demand\_avg\_miss\_latency::.cpu.inst 41727.407473 # average overall miss latency

system.cpu.icache.demand\_avg\_miss\_latency::total 41727.407473 # average overall miss latency

system.cpu.icache.overall\_avg\_miss\_latency::.cpu.inst 41727.407473 # average overall miss latency

system.cpu.icache.overall\_avg\_miss\_latency::total 41727.407473 # average overall miss latency

system.cpu.icache.blocked\_cycles::no\_mshrs 0 # number of cycles access was blocked

system.cpu.icache.blocked\_cycles::no\_targets 0 # number of cycles access was blocked

system.cpu.icache.blocked::no\_mshrs 0 # number of cycles access was blocked

system.cpu.icache.blocked::no\_targets 0 # number of cycles access was blocked

system.cpu.icache.avg\_blocked\_cycles::no\_mshrs nan # average number of cycles each access was blocked

system.cpu.icache.avg\_blocked\_cycles::no\_targets nan # average number of cycles each access was blocked

system.cpu.icache.writebacks::.writebacks 2784525 # number of writebacks

system.cpu.icache.writebacks::total 2784525 # number of writebacks

system.cpu.icache.ReadReq\_mshr\_misses::.cpu.inst 2785036 # number of ReadReq MSHR misses

system.cpu.icache.ReadReq\_mshr\_misses::total 2785036 # number of ReadReq MSHR misses

system.cpu.icache.demand\_mshr\_misses::.cpu.inst 2785036 # number of demand (read+write) MSHR misses

system.cpu.icache.demand\_mshr\_misses::total 2785036 # number of demand (read+write) MSHR misses

system.cpu.icache.overall\_mshr\_misses::.cpu.inst 2785036 # number of overall MSHR misses

system.cpu.icache.overall\_mshr\_misses::total 2785036 # number of overall MSHR misses

system.cpu.icache.ReadReq\_mshr\_miss\_latency::.cpu.inst 113427297000 # number of ReadReq MSHR miss cycles

system.cpu.icache.ReadReq\_mshr\_miss\_latency::total 113427297000 # number of ReadReq MSHR miss cycles

system.cpu.icache.demand\_mshr\_miss\_latency::.cpu.inst 113427297000 # number of demand (read+write) MSHR miss cycles

system.cpu.icache.demand\_mshr\_miss\_latency::total 113427297000 # number of demand (read+write) MSHR miss cycles

system.cpu.icache.overall\_mshr\_miss\_latency::.cpu.inst 113427297000 # number of overall MSHR miss cycles

system.cpu.icache.overall\_mshr\_miss\_latency::total 113427297000 # number of overall MSHR miss cycles

system.cpu.icache.ReadReq\_mshr\_miss\_rate::.cpu.inst 0.018949 # mshr miss rate for ReadReq accesses

system.cpu.icache.ReadReq\_mshr\_miss\_rate::total 0.018949 # mshr miss rate for ReadReq accesses

system.cpu.icache.demand\_mshr\_miss\_rate::.cpu.inst 0.018949 # mshr miss rate for demand accesses

system.cpu.icache.demand\_mshr\_miss\_rate::total 0.018949 # mshr miss rate for demand accesses

system.cpu.icache.overall\_mshr\_miss\_rate::.cpu.inst 0.018949 # mshr miss rate for overall accesses

system.cpu.icache.overall\_mshr\_miss\_rate::total 0.018949 # mshr miss rate for overall accesses

system.cpu.icache.ReadReq\_avg\_mshr\_miss\_latency::.cpu.inst 40727.407832 # average ReadReq mshr miss latency

system.cpu.icache.ReadReq\_avg\_mshr\_miss\_latency::total 40727.407832 # average ReadReq mshr miss latency

system.cpu.icache.demand\_avg\_mshr\_miss\_latency::.cpu.inst 40727.407832 # average overall mshr miss latency

system.cpu.icache.demand\_avg\_mshr\_miss\_latency::total 40727.407832 # average overall mshr miss latency

system.cpu.icache.overall\_avg\_mshr\_miss\_latency::.cpu.inst 40727.407832 # average overall mshr miss latency

system.cpu.icache.overall\_avg\_mshr\_miss\_latency::total 40727.407832 # average overall mshr miss latency

system.cpu.icache.replacements 2784525 # number of replacements

system.membus.snoop\_filter.tot\_requests 5574367 # Total number of requests made to the snoop filter.

system.membus.snoop\_filter.hit\_single\_requests 2786429 # Number of requests hitting in the snoop filter with a single holder of the requested data.

system.membus.snoop\_filter.hit\_multi\_requests 0 # Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data.

system.membus.snoop\_filter.tot\_snoops 0 # Total number of snoops made to the snoop filter.

system.membus.snoop\_filter.hit\_single\_snoops 0 # Number of snoops hitting in the snoop filter with a single holder of the requested data.

system.membus.snoop\_filter.hit\_multi\_snoops 0 # Number of snoops hitting in the snoop filter with multiple (>1) holders of the requested data.

system.membus.pwrStateResidencyTicks::UNDEFINED 364964286500 # Cumulative time (in ticks) in various power states

system.membus.trans\_dist::ReadResp 2787634 # Transaction distribution

system.membus.trans\_dist::WritebackDirty 336 # Transaction distribution

system.membus.trans\_dist::WritebackClean 2784525 # Transaction distribution

system.membus.trans\_dist::CleanEvict 1567 # Transaction distribution

system.membus.trans\_dist::ReadExReq 304 # Transaction distribution

system.membus.trans\_dist::ReadExResp 304 # Transaction distribution

system.membus.trans\_dist::ReadCleanReq 2785036 # Transaction distribution

system.membus.trans\_dist::ReadSharedReq 2599 # Transaction distribution

system.membus.pkt\_count\_system.cpu.icache.mem\_side::system.mem\_ctrls.port 8354596 # Packet count per connected master and slave (bytes)

system.membus.pkt\_count\_system.cpu.dcache.mem\_side::system.mem\_ctrls.port 7709 # Packet count per connected master and slave (bytes)

system.membus.pkt\_count::total 8362305 # Packet count per connected master and slave (bytes)

system.membus.pkt\_size\_system.cpu.icache.mem\_side::system.mem\_ctrls.port 356451840 # Cumulative packet size per connected master and slave (bytes)

system.membus.pkt\_size\_system.cpu.dcache.mem\_side::system.mem\_ctrls.port 207296 # Cumulative packet size per connected master and slave (bytes)

system.membus.pkt\_size::total 356659136 # Cumulative packet size per connected master and slave (bytes)

system.membus.snoops 0 # Total snoops (count)

system.membus.snoopTraffic 0 # Total snoop traffic (bytes)

system.membus.snoop\_fanout::samples 2787939 # Request fanout histogram

system.membus.snoop\_fanout::mean 0.000000 # Request fanout histogram

system.membus.snoop\_fanout::stdev 0.000599 # Request fanout histogram

system.membus.snoop\_fanout::underflows 0 0.00% 0.00% # Request fanout histogram

system.membus.snoop\_fanout::0 2787938 100.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::1 1 0.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::2 0 0.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::overflows 0 0.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::min\_value 0 # Request fanout histogram

system.membus.snoop\_fanout::max\_value 1 # Request fanout histogram

system.membus.snoop\_fanout::total 2787939 # Request fanout histogram

system.membus.reqLayer0.occupancy 17117422000 # Layer occupancy (ticks)

system.membus.reqLayer0.utilization 4.7 # Layer utilization (%)

system.membus.respLayer1.occupancy 14256458241 # Layer occupancy (ticks)

system.membus.respLayer1.utilization 3.9 # Layer utilization (%)

system.membus.respLayer2.occupancy 15855000 # Layer occupancy (ticks)

system.membus.respLayer2.utilization 0.0 # Layer utilization (%)

---------- End Simulation Statistics ----------